Santa Ana, CA
Microsemi
Progress Powered by Technology

2830 S. Fairview St.
Santa Ana, CA 92704
PH: (714) 979-8220
FAX: (714) 966-5256

MSAHX75L60C

Features

- Rugged polysilicon gate cell structure
- high current handling capability, latch-proof
- Hermetically sealed, surface mount power package
- Low package inductance
- Very low thermal resistance
- Reverse polarity available upon request: MSAHX75L60D
- low VCE(sat) IGBT, low conduction losses

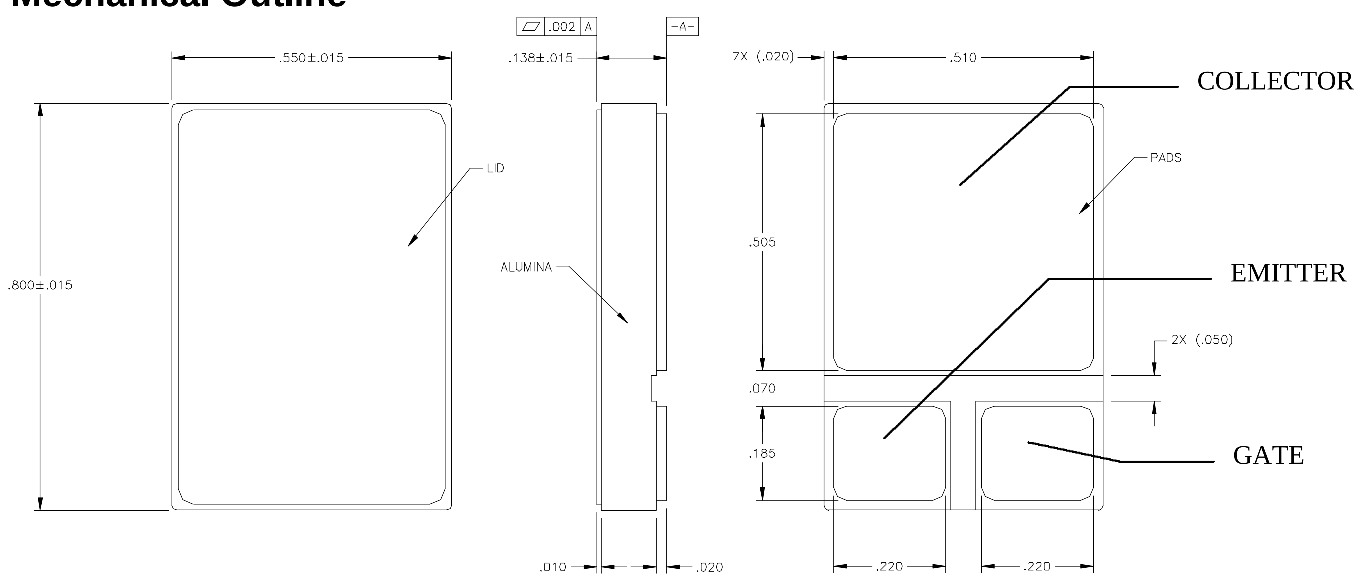
600 Volts
75 Amps
1.8 Volts vce(sat)

N-CHANNEL INSULATED GATE BIPOLAR TRANSISTOR

Maximum Ratings @ 25°C (unless otherwise specified)

DESCRIPTION	SYMBOL	MAX.	UNIT
Collector-to-Emitter Breakdown Voltage (Gate Shorted to Emitter) @ $T_J \geq 25°C$	BV_{CES}	600	Volts
Collector-to-Gate Breakdown Voltage @ $T_J \geq 25°C$, R_{GS}= 1 MΩ	BV_{CGR}	600	Volts
Continuous Gate-to-Emitter Voltage	V_{GES}	+/-20	Volts
Transient Gate-to-Emitter Voltage	V_{GEM}	+/-30	Volts
Continuous Collector Current Tj= 25°C Tj= 90°C	I_{C25} I_{C90}	75 60	Amps
Peak Collector Current, pulse width limited by T_{jmax},	I_{CM}	200	Amps
Safe Operating Area (RBSOA) @ V_{GE}= 15V, L= 30μH (clamped inductive load), R_G= 2.7Ω, Tj= 125°C, V_{CE}= 0.8 x V_{CES}	I_{max}	100	Amps
Power Dissipation	P_D	300	Watts
Junction Temperature Range	T_j	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	0.25	°C/W

Mechanical Outline



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Electrical Parameters @ 25°C (unless otherwise specified)

DESCRIPTION	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNIT
Collector-to-Emitter Breakdown Voltage (Gate Shorted to Emitter)	BV_{CES}	V_{GS} = 0 V, I_C = 250 µA	600			V
Gate Threshold Voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 250 µA	2.5		5.0	V
Gate-to-Emitter Leakage Current	I_{GES}	V_{GE} = ± 20V_{DC}, V_{CE} = 0 T_J = 25°C T_J = 125°C			±100 ±200	nA
Collector-to-Emitter Leakage Current (Zero Gate Voltage Collector Current)	I_{CES}	V_{CE} =0.8•BV_{CES} T_J = 25°C V_{GE} = 0 V T_J = 125°C			200 1000	µA
Collector-to-Emitter Saturation Voltage (1)	$V_{CE(sat)}$	V_{GE}= 15V, I_C= 60A T_J = 25°C I_C= 60A T_J = 125°C		 1.8	1.8	V
Forward Transconductance (1)	g_{fs}	V_{CE} ≥ 10 V; I_C = 60 A	30	40		S
Input Capacitance Output Capacitance Reverse Transfer Capacitance	C_{ies} C_{oes} C_{res}	V_{GE} = 0 V, V_{CE} = 25 V, f = 1 MHz		4000 340 100		pF
INDUCTIVE LOAD, Tj= 25°C Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time Off Energy	 $t_{d(on)}$ t_{ri} $t_{d(off)}$ t_{fi} E_{off}	V_{GE} = 15 V, V_{CE} = 480 V, I_C = 60 A, R_G = 2.7 Ω, L= 100 µH note 2, 3		 50 210 600 500 16	 800 700 	 ns ns ns ns mJ
INDUCTIVE LOAD, Tj= 125°C Turn-on Delay Time Rise Time On Energy Turn-off Delay Time Fall Time Off Energy	 $t_{d(on)}$ t_{ri} E_{on} $t_{d(off)}$ t_{fi} E_{off}	V_{GE} = 15 V, V_{CE} = 480 V, I_C = 60 A, R_G = 2.7 Ω, L= 100 µH note 2, 3		 50 240 3 1000 1000 26		 ns ns mJ ns ns mJ
Total Gate Charge Gate-to-Emitter Charge Gate-to-Collector (Miller) Charge	Q_g Q_{ge} Q_{gc}	V_{GE} = 15 V, V_{CE} = 300V, I_C = 50A		200 35 80	250 50 100	nC
Antiparallel diode forward voltage	V_F	I_E= 30 A T_J = 25 °C I_E= 60 A T_J = 25 °C I_E= 100 A T_J = 25 °C I_E= 60 A T_J = 150 °C		1.55 1.75 2 1.5		V V V V
Antiparallel diode reverse recovery time	t_{rr}	I_E= 1 A, dI_E/dt= 100 A/us, T_J= 25°C I_E= 10 A, dI_E/dt= 200 A/us, T_J= 100°C I_E= 40 A, dI_E/dt= 200 A/us, T_J= 100°C		35 120 140	 150 	ns ns ns
Antiparallel diode reverse recovery charge	Q_{rr}	I_E= 10 A, dI_E/dt= 200 A/us, T_J= 100°C I_E= 40 A, dI_E/dt= 100 A/us, T_J= 100°C		500 750		nC nC
Antiparallel diode peak recovery current	I_{RM}	I_E= 10 A, dI_E/dt= 200 A/us, T_J= 100°C I_E= 40 A, dI_E/dt= 200 A/us, T_J= 100°C		7 9		A A

Notes

(1) Pulse test, t ≤ 300 µs, duty cycle δ ≤ 2%
(2) switching times and losses may increase for larger V_{CE} and/or R_G values or higher junction temperatures.
(3) switching losses include "tail" losses
(4) Microsemi Corp. does not manufacture the igbt die; contact company for details.